Claims

[c1] A method for implementing dual damascene processing, the method comprising:
forming a first hardmask layer over an interlevel dielectric layer;
forming a second hardmask layer over said first hardmask layer;
opening a trench pattern within a third hardmask layer formed over said second hardmask;
implementing a first etch process so as to define a via pattern completely through said second hardmask layer and partially through said first hardmask layer; and
implementing a second etch process to transfer said trench pattern and said via pattern into said interlevel dielectric layer.

[c2] The method of claim 1, wherein said interlevel dielectric layer is selected from a material having a faster etch rate with respect to said first and said second hardmask layers.

[c3] The method of claim 1, wherein said first etch process is implemented with a first etch chemistry such that said second hardmask layer etches at a faster rate with re-

spect to said first hardmask layer.

[c4] The method of claim 3, wherein said first hardmask layer comprises a low-k dielectric barrier, and said second hardmask comprises silicon nitride.

[c5] The method of claim 1, wherein said second etch process is implemented with a second etch chemistry such that said second hardmask layer etches at about an equal rate with respect to said first hardmask layer.

[c6] The method of claim 2, wherein said interlevel dielectric layer further comprises an organic, low-k material.

[c7] The method of claim 2, wherein said interlevel dielectric layer further comprises a porous, organosilciate (OSG) type material.

[c8] A method for implementing dual damascene processing for a semiconductor device, the method comprising:
forming a first hardmask layer over an interlevel dielectric layer;
forming a second hardmask layer over said first hardmask layer;
opening a trench pattern within a third hardmask layer formed over said second hardmask;
implementing a first etch process so as to define a via pattern completely through said second hardmask layer

and partially through said first hardmask layer;
stripping a photoresist layer used to create said via pattern; and
following said stripping, implementing a second etch process to transfer said trench pattern and said via pattern into said interlevel dielectric layer.

[c9] The method of claim 8, wherein said interlevel dielectric layer is selected from a material having a faster etch rate with respect to said first and said second hardmask layers.

[c10] The method of claim 8, wherein said first etch process is implemented with a first etch chemistry such that said second hardmask layer etches at a faster rate with respect to said first hardmask layer.

[c11] The method of claim 10, wherein said first hardmask layer comprises a low-k dielectric barrier, and said second hardmask comprises silicon nitride.

[c12] The method of claim 8, wherein said second etch process is implemented with a second etch chemistry such that said second hardmask layer etches at about an equal rate with respect to said first hardmask layer.

[c13] The method of claim 9, wherein said interlevel dielectric layer further comprises an organic, low-k material.

[c14] The method of claim 9, wherein said interlevel dielectric layer further comprises a porous, organosilciate (OSG) type material.

[c15] The method of 12, wherein during said second etch said via pattern is extended by at least about 60% into the thickness of said interlevel dielectric layer at a point when exposed portions of said first and said second hardmask layers are completely removed.

[c16] The method of claim 15, wherein a resulting trench depth formed in said interlevel dielectric layer is about 35% to about 40% of said thickness of said interlevel dielectric layer once said via pattern reaches a cap layer beneath said interlevel dielectric layer.